046246 (08) 5348164 September 20, 1994

UNITED STATES PATENT AND TRADEMARK OFFICE GRANTED PATENT

5348164

September 20, 1994

Method and apparatus for testing integrated circuits

REISSUE: Reissue Application filed Sep. 19, 1996 (O.G. Feb. 11, 1997) Ex. Gp.: 3101; Re. S.N. 08/715,869, (O.G. February 11, 1997)

INVENTOR: Heppler, Steve W., Kuna, ID

APPL-NO: 046246 (08)

FILED-DATE: April 13, 1993

GRANTED-DATE: September 20, 1994

ASSIGNEE-AT-ISSUE: Micron Semiconductor, Inc., Boise, ID

ASSIGNEE-AFTER-ISSUE: April 13, 1993 - ASSIGNMENT OF ASSIGNORS INTEREST., MICRON SEMICONDUCTOR, INC. PATENT DEPART. MAIL STOP 507 2805 E. COLOMBIA ROAD BOISE IDAHO 83706, Reel and Frame Number: 006520/0482
September 12, 1994 - NONE CORRECTED ASSIGNMENT: REEL: 6520 FRAME: 0482, MICRON SEMICONDUCTOR, INC. PATENT DEPT. MS507 2805 EAST COLUMBIA ROAD B OISE, ID 83706, Reel and Frame Number: 007125/0785

LEGAL-REP: Starkweather, Michael W.

REF-CITED:
4691831, 1987, United States (US)
4733459, 1988, United States (US)
4805779, 1989, United States (US)
4976356, 1990, United States (US)
5230432, 1993, United States (US)
5261775, 1993, United States (US)
5527955, Japan (JP)

ENGLISH-ABST:

There is an IC (integrated circuit) testing device 11 that receives singulated ICs from a singulation station's bottom table 44, where an IC 15 has slid down onto loading ramp or track 16. The IC will slide into test station 18, where stop pin 22 has been inserted to stop the IC in DUT (device under test) station

20. In the DUT station, the IC is securely held in position by an extractor bar 26, insertion bar 28, and a part guide 24. Thereby, test cite station 18 will move downward and insert IC 15 into testing socket 30. After testing the IC, testing station 18 returns upward with the IC in the same secured position. Pin 22 will be removed to allow the IC to slide into part holding station 31. If the IC was not defective, pin 32 will be removed to allow the IC to slide onto track 36 of the IC separator station 34. While the test cite station 18 is in the up position a second IC is slid along track 16 and loaded into DUT cite 20 being readied for the next test cycle. However, if the first IC was found to be defective, pin 32 will be positioned so as to stop the IC from sliding onto track 36. Thereby, the test cite 18 will proceed to the down position to test the second IC, and simultaneously pin 32 will be removed to now allow the defective IC to slide onto track 38. The second IC has now completed its testing and is ready to proceed to the remainder of the cycle.

Patent, Trademarks Copyright Periodicals, Combined

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Patent Number :

US5348164 A 19940920 [US5348164]

Title :

(A) Method and apparatus for testing integrated circuits

Patent Assignee :

(A) MICRON SEMICONDUCTOR INC (US)

Patent Assignee :

Micron Semiconductor, Inc., Boise ID [US]

Inventor(s) :

(A) HEPPLER STEVE W (US)

Application Nbr :

US4624693 19930413 [1993US-0046246]

Priority Details :

US4624693 19930413 [1993US-0046246]

Intl Patent Class :

(A) B07C-005/344

EPO ECLA Class :

B07C-005/344
G01R-031/316B
H05K-013/02B

US Patent Class :

ORIGINAL (O) : 209573000; CROSS-REFERENCE (X) : 209911000
324158100

Document Type :

Basic

Citations :

US4691831; US4733459; US4805779; US4976356; US5230432;
US5261775; JP55-27955
Welcon Sockets and Connectors, Wells Electronics, Inc. 1701 S. Main St.,
South Bend, Ind., 46613 1991.

Publication Stage :

(A) United States patent

Abstract :

There is an IC (integrated circuit) testing device 11 that receives singulated

ICs from a singulation station's bottom table 44, where an IC 15 has slid down onto loading ramp or track 16. The IC will slide into test station 18, where stop pin 22 has been inserted to stop the IC in DUT (device under test) station 20. In the DUT station, the IC is securely held in position by an extractor bar 26, insertion bar 28, and a part guide 24. Thereby, test cite station 18 will move downward and insert IC 15 into testing socket 30. After testing the IC, testing station 18 returns upward with the IC in the same secured position. Pin 22 will be removed to allow the IC to slide into part holding station 31. If the IC was not defective, pin 32 will be removed to allow the IC to slide onto track 36 of the IC separator station 34. While the test cite station 18 is in the up position a second IC is sl! id along track 16 and loaded into DUT cite 20 being readied for the next test cycle. However, if the first IC was found to be defective, pin 32 will be positioned so as to stop the IC from sliding onto track 36. Thereby, the test cite 18 will proceed to the down position to test the second IC, and simultaneously pin 32 will be removed to now allow the defective IC to slide onto track 38. The second IC has now completed its testing and is ready to proceed to the remainder of the cycle.

Patent Number :

US5348164 A 19940920 [US5348164]

Application Number :

US4624693 19930413 [1993US-0046246]

Action Taken :

19930413 US/AS02-A
ASSIGNMENT OF ASSIGNOR'S INTEREST
OWNER: MICRON SEMICONDUCTOR, INC. PATENT DEPART. MAIL STO; EFFECTIVE DATE: 19930409

19930413 US/AS02-A
ASSIGNMENT OF ASSIGNOR'S INTEREST
OWNER: HEPPLER, STEVE W.; EFFECTIVE DATE: 19930409

19940912 US/AS28-A
CORRECTED ASSIGNMENT
MICRON SEMICONDUCTOR, INC. PATENT DEPT. MS507 2805 EAST COLUMBIA ROAD BOISE, ID * HEPPLER, STEVE W.: 19930409

19970211 US/RF-A
REISSUE APPLICATION FILED
EFFECTIVE DATE: 19960919

Update Code :

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1 / 1 CRXX - ©CLAIMS/RRX

Patent Number :

5,348,164 A 19940920 [US5348164]

Patent Assignee :

Micron Semiconductor Inc

Actions :

19960919 REISSUE REQUESTED
Issue Date of O.G.: 19970211
Reissue Request Number: 08/715869
Examination Group responsible for Reissue process: 3101

Query/Command : file inpadoc

Query/Command : us5348164/pn

**** SS 3: Results 1**
Search statement 4

Query/Command : PRT SS 3 MAX 1 LEGAL

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1 / 1 INPADOC - ©INPADOC

Patent Number :

US 5348164 A 19940920 [US5348164]

Title :

METHOD AND APPARATUS FOR TESTING INTEGRATED CIRCUITS

Inventor(s) :

HEPPLER STEVE W [US]

Patent Assignee (Words) :

MICRON SEMICONDUCTOR INC [US]

Application Details :

US 46246/93-A 19930413 [1993US-0046246]

Priority Details :

US 46246/93-A 19930413 [1993US-0046246]

Intl. Patent Class. :

B07C-005/344

WPI Cross Reference :

1994-301834 (G)

1/1 LGST - ©EPO

Patent Number :

US5348164 A 19940920 [US5348164]

Application Number :

US4624693 19930413 [1993US-0046246]

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19970211 US/RF-A
REISSUE APPLICATION FILED
EFFECTIVE DATE: 19960919

Update Code :

2003-22

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